

FIG. 1

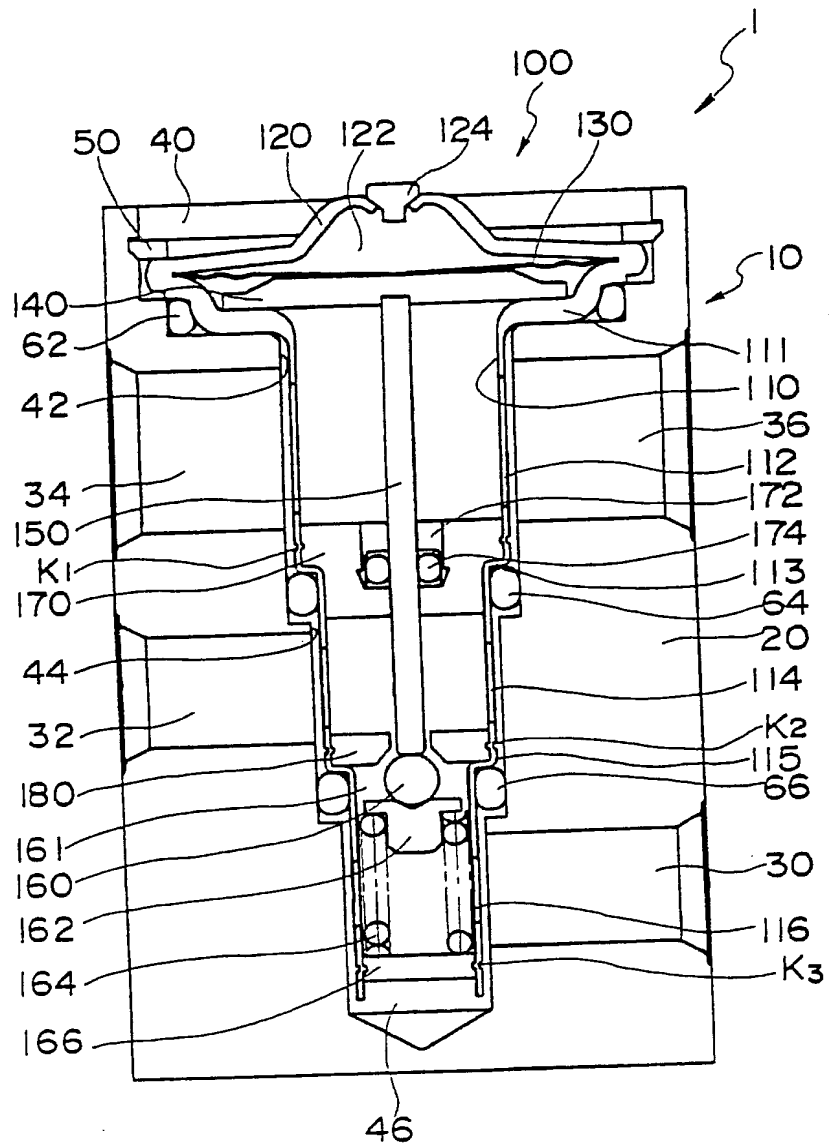


FIG. 2

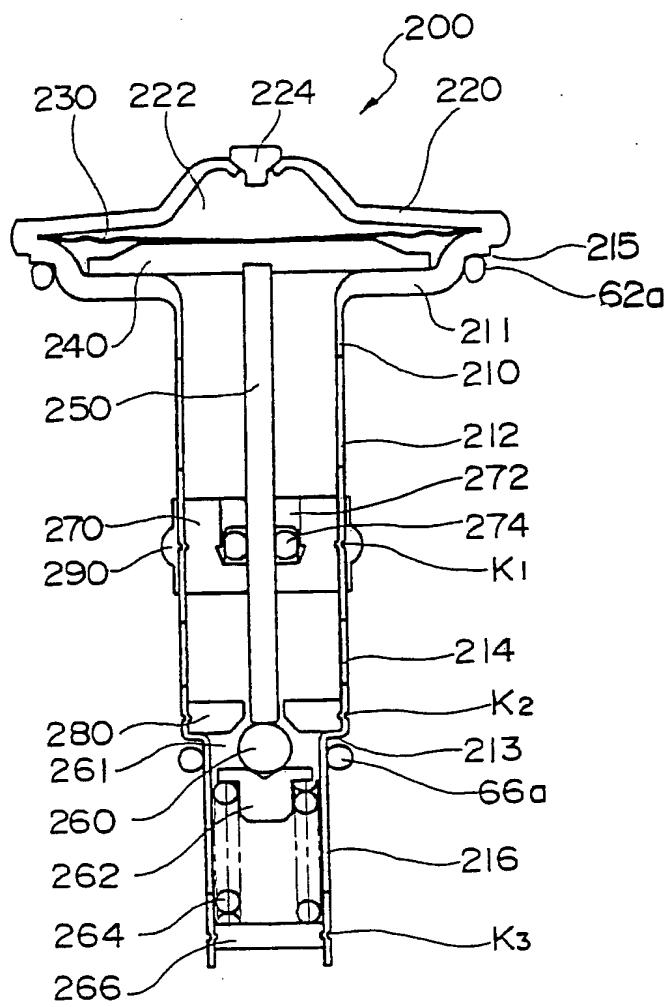


FIG. 3

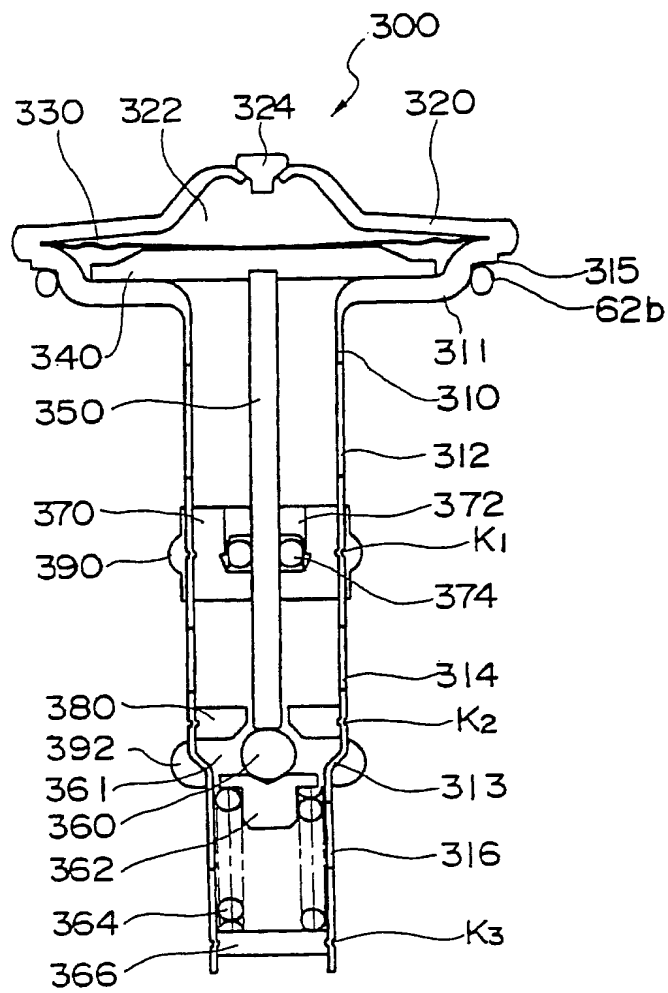
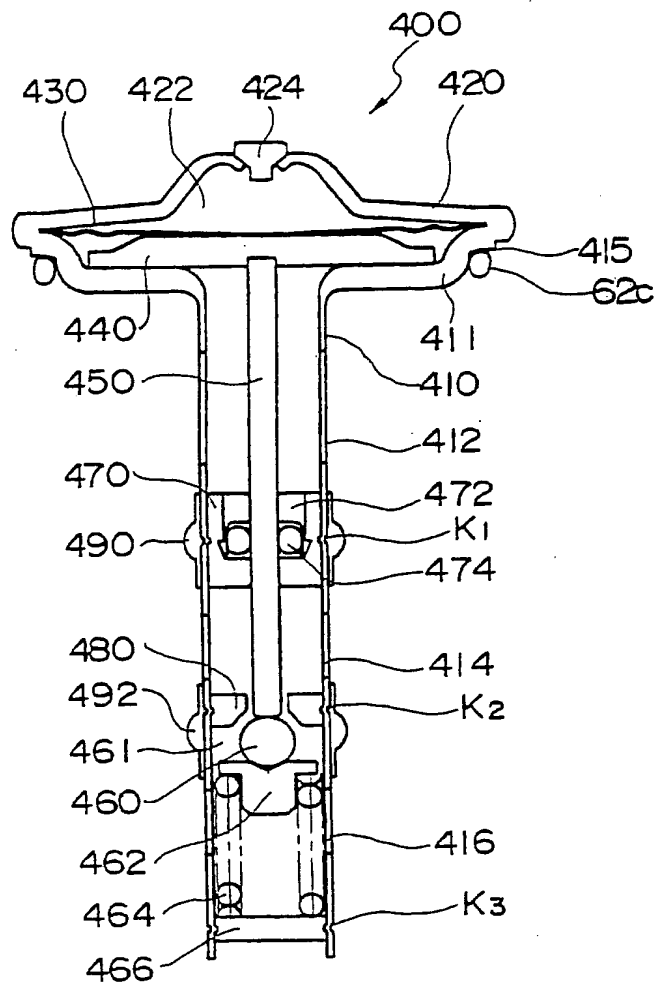
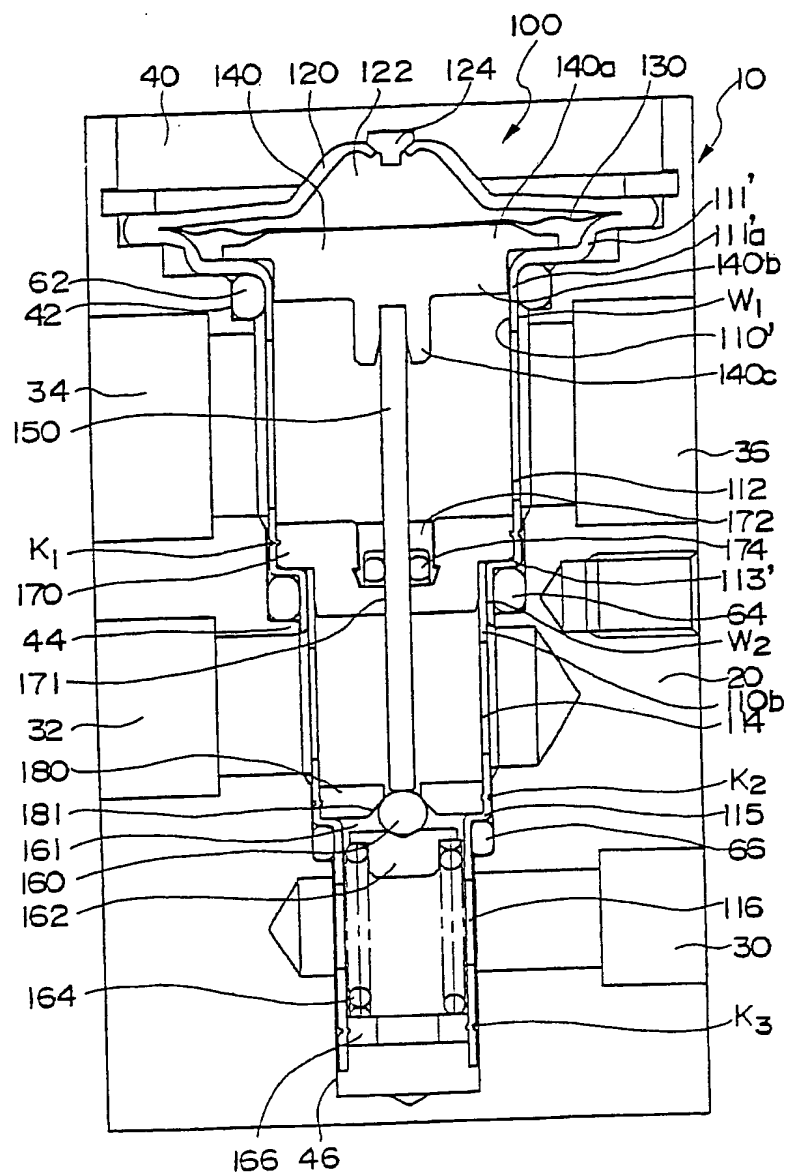


FIG. 4

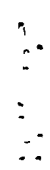


A detailed cross-sectional diagram of a semiconductor device. The device features a central vertical channel or well structure. At the top, there are several horizontal layers and structures, including what appears to be a gate stack or contact layer (labeled 40, 120, 122, 124) and a source/drain region (100). Below these, the central channel is defined by insulating or doped regions (130, 140a, 140b, 140c). Various other components are shown, such as spacers (62, 42), gates (34, 150), and different material layers (K1, W1, 110', 111', 112, 172, 174, 113, 64, 20, 114, K2, 115, 66, 116, 30, K3). The bottom of the device shows additional layers and contacts (166, 46). The entire structure is enclosed within a substrate or package frame.

FIG. 6



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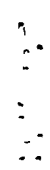


FIG. 9

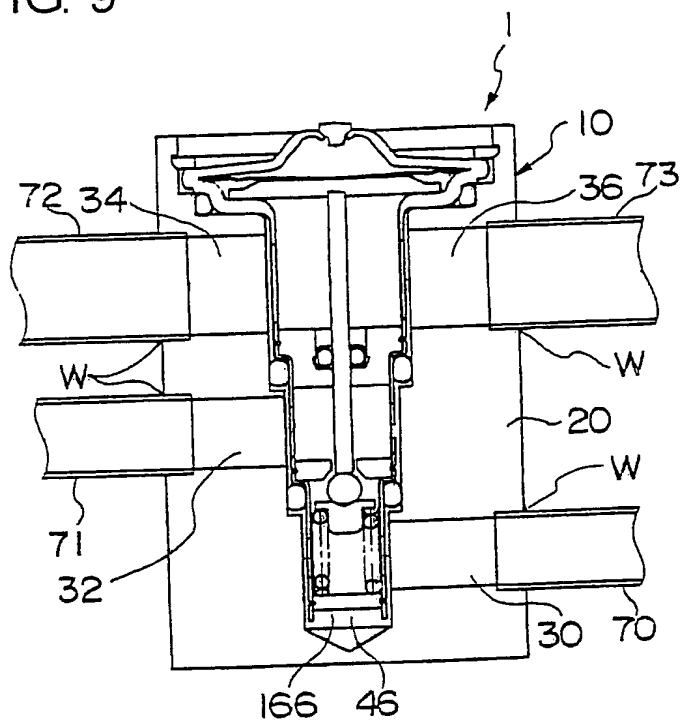


FIG. 10

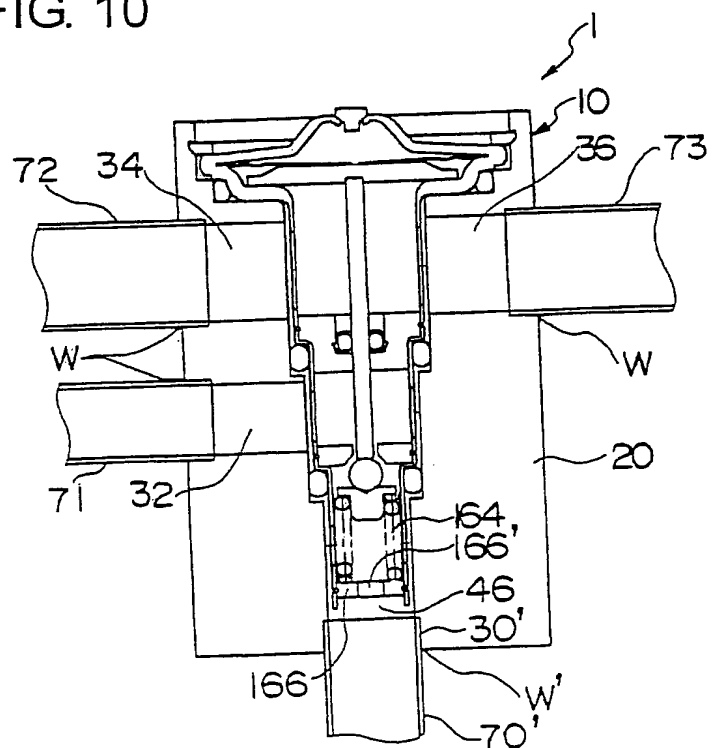




FIG. 11

